

Application number 09/837,897  
Amendment dated November 3, 2004  
Reply to office action mailed May 5, 2004

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

**Claims 1-17 (Cancelled)**

**Claim 18 (Currently amended) An integrated circuit comprising:**

a voltage controlled oscillator comprising:

a first gm cell;

a second gm cell having a noninverting input coupled to a noninverting output of the first gm cell, an inverting input coupled to an inverting output of the first gm cell, a noninverting output coupled to an inverting input of the first gm cell, and an inverting output coupled to a noninverting input of the first gm cell;

a first capacitance coupled between the noninverting output and inverting output of the first gm cell;

a second capacitance coupled between the noninverting output and inverting output of the second gm cell; and

a first filter comprising:

a third gm cell,

wherein the first gm cell, the second gm cell, and the third gm cell each comprise a variable resistance, the variable resistance comprising a native MOS device.

**Claim 19 (Previously presented) The integrated circuit of claim 18 wherein the variable resistance comprises a plurality of native MOS devices coupled in series.**

**Claim 20 (Previously presented) The integrated circuit of claim 18 wherein the variable resistance comprises two native MOS devices coupled in series.**

**Claim 21 (Previously presented) The integrated circuit of claim 18 wherein a gate of the native MOS device is configured to receive a control voltage.**

Application number 09/837,897  
Amendment dated November 3, 2004  
Reply to office action mailed May 5, 2004

PATENT

**Claim 22 (Previously presented)** The integrated circuit of claim 21 further comprising:

a phase/frequency detector having an input coupled to the voltage controlled oscillator; and

a charge pump coupled between the phase/frequency detector and the voltage controlled oscillator.

**Claim 23 (Currently amended)** The integrated circuit of claim 22 further comprising a loop filter coupled to an output of the charge pump,

wherein the loop filter is configured to provide a the control voltage to the voltage controlled oscillator.

**Claim 24 (Currently amended)** The integrated circuit of claim 23 wherein the control voltage is used to tune a the first filter.

**Claim 25 (Currently amended)** The integrated circuit of claim 24 wherein the first filter is a low pass filter.

**Claim 26 (Previously presented)** A method of tuning a filter comprising:  
receiving a reference clock signal having a first frequency;  
receiving a signal having a second frequency from a voltage controlled oscillator;  
comparing the first frequency to the second frequency;  
providing a charging signal to a loop filter, the charging signal based on the comparison between the first frequency and the second frequency; and  
adjusting the second frequency by:  
receiving an output signal from the loop filter; and  
using the output signal from the loop filter to adjust a first variable resistance, wherein the first variable resistance is included in a first gm cell in the voltage controlled oscillator, and the first variable resistance comprises a first native MOS device.

**Claim 27 (Previously presented)** The method of claim 26 further comprising:

Application number 09/837,897  
Amendment dated November 3, 2004  
Reply to office action mailed May 5, 2004

PATENT

receiving the output signal from the loop filter with a second filter;  
using the output signal from the loop filter to adjust a second variable resistance,  
wherein the second variable resistance is included in a second gm cell, and the  
second variable resistance comprises a second native MOS device,  
wherein a value of the second variable resistance determines a frequency  
characteristic of the second filter.

**Claim 28 (Previously presented)** The method of claim 27 wherein the second  
filter is a low pass filter.

**Claim 29 (Previously presented)** The method of claim 28 wherein the  
frequency characteristic of the second filter is a cutoff frequency of the second filter.

**Claim 30 (previously presented)** The integrated circuit of claim 29 wherein  
the second variable resistance comprises a plurality of native MOS devices coupled in series.

**Claim 31 (previously presented)** The integrated circuit of claim 29 wherein  
the second variable resistance comprises two native MOS devices coupled in series.

**Claim 32 (previously presented)** An integrated circuit comprising:  
a phase-locked loop configured to tune a filter and comprising:  
a phase/frequency detector having a first input, and a second input  
configured to receive a reference clock;  
a charge pump coupled to an output of the phase/frequency detector; and  
a voltage controlled oscillator having an control voltage input coupled to  
an output of the charge pump and an output coupled to the first input of the phase/frequency  
detector, the voltage controlled oscillator comprising:

a first gm cell;  
a second gm cell having a noninverting input coupled to a  
noninverting output of the first gm cell, an inverting input coupled to an inverting output of the

Application number 09/837,897  
Amendment dated November 3, 2004  
Reply to office action mailed May 5, 2004

PATENT

first gm cell, a noninverting output coupled to an inverting input of the first gm cell, and an inverting output coupled to a noninverting input of the first gm cell;  
a first capacitance coupled between the noninverting and inverting outputs of the first gm cell;

a second capacitance coupled between the noninverting and inverting outputs of the second gm cell; and

a first filter having a control voltage input coupled to the output of the charge pump and comprising a third gm cell,

wherein the first gm cell, the second gm cell, and the third gm cell each comprise a variable resistance, the variable resistance comprising a native MOS device.

**Claim 33 (Previously presented)** The integrated circuit of claim 32 wherein the phase-locked loop further comprises a loop filter configured to filter the output of the charge pump.

**Claim 34 (Previously presented)** The integrated circuit of claim 32 wherein the variable resistance comprises a plurality of native MOS devices coupled in series.

**Claim 35 (Previously presented)** The integrated circuit of claim 32 wherein the variable resistance comprises two native MOS devices coupled in series.

**Claim 36 (Previously presented)** The integrated circuit of claim 35 wherein a gate of the native MOS devices are configured to receive the output of the charge pump.

**Claim 37 (Previously presented)** The method of claim 36 wherein the first filter is a low pass filter.